AMENDMENTS TO THE CLAIMS

1. (currently amended) A trench corner effect, bidirectional flash memory cell comprising:

a trench formed in a silicon substrate;

at least a corner of a first and second side of the trench having a trapping material comprising an oxide-nitride-oxide architecture;

an oxide material filling the trench;

a plurality of active areas located in the silicon substrate substantially adjacent to the first and second sides; and

a control gate above the trench.

2. (canceled)

3. (Original) The memory cell of claim 1 wherein the trapping material is deposited on the first and second sides of the trench.

4. (Original) The memory cell of claim 1 wherein the trapping material traps electrons.

5. (Original) The memory cell of claim 1 wherein the control gate overlaps at least a portion of each active area.

6. (Original) The memory cell of claim 1 wherein a first active area of the plurality of active areas is a drain area and a second active area is a source area.

7. (Previously Presented) A trench corner effect, bidirectional flash memory cell comprising:

a trench formed in a silicon substrate;

an oxide material filling the trench;

a first and second side of the trench comprising a trapping material between the oxide material and the silicon substrate;

a drain region located in the silicon substrate substantially adjacent to the first side of the trench near the trapping material;

a source region located in the silicon substrate substantially adjacent to the second side of the trench near the trapping material; and

a control gate over the trench such that the control gate and oxide material overlap at least a portion of the drain and source regions.

8. (Original) The memory cell of claim 7 wherein the substrate is comprised of a p-type conductive material and the drain and source regions are comprised of an n-type conductive material.

9. (Original) The memory cell of claim 7 wherein the substrate is comprised of an n-type conductive material and the drain and source regions are comprised of a p-type conductive material.

10. (Original) The memory cell of claim 7 wherein the trapping material on the first side stores a first data bit and the trapping material on the second side stores a second data bit.

11 – 24 (Canceled)

25. (Previously Presented) A trench corner effect, bidirectional flash memory cell comprising:

a trench formed in a silicon substrate;

a low-trap-density dielectric material substantially filling the trench;

a trapping material formed in a first and second corner of the trench between the dielectric material and the silicon substrate such that a first trapping area is formed in the first corner and a second trapping area is formed in the second corner;

drain and source regions located in the silicon substrate, each region substantially adjacent to either the first or the second side; and

a control gate formed over the trench such that the control gate and dielectric material overlap at least a portion of the drain and source regions.

26. (Previously Presented) The memory cell of claim 25 wherein direction of operation of the memory cell determines which side of the trench is adjacent to the drain region and which side is adjacent to the source region.

27. (Previously Presented) The memory cell of claim 25 wherein the trapping material is formed along the bottom of the trench between the first and second corners.

28. (Previously Presented) The memory cell of claim 27 wherein the thickness of the trapping layer formed along the bottom of the trench is such that the first and second trapping areas are isolated from each other.

29. (Previously Presented) The memory cell of claim 25 wherein the trapping material forms a continuous layer along the inside of the trench.

30. (Previously Presented) The memory cell of claim 25 wherein the cell is an n-channel device such that the first and second trapping areas are hole trapping areas.

31. (Previously Presented) The memory cell of claim 25 wherein the cell is a p-channel device such that the first and second trapping areas are electron trapping areas.

32. (Previously Presented) The memory cell of claim 25 wherein the trench extends into the silicon substrate at least as deep as the drain and source regions.

33. (Previously Presented) The memory cell of claim 25 wherein the trapping material is substantially confined to only the first and second corners of the trench.

34. (Previously Presented) The memory cell of claim 25 wherein the trapping material has an oxide-nitride-oxide structure.